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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PLANTE, JONATHAN R	
ART UNIT	PAPER NUMBER
2112	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/711,000	Applicant(s) TSAI ET AL.	
	Examiner Jonathan R. Plante	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application Number: 10/711,000 filed on 17 August 2004 has a total of 20 claims pending in the application; there are 3 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/711,000, filed on 05 September 2004. Applicant is granted the date of 30 December 2003 for priority.

Drawings

4. The drawings are objected to because:

   a. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

   b. Please label index 208 on Figure 3 as "Computer system".

   c. Please label index 210 on Figure 3 as "Real input device".

d. Please label index 212 on Figure 3 as "Emulation input device".

e. Please place a dashed box around Figure 3 to represent Figure 3 as "Switch device" from Figure 2 index 202 and label place appropriate label for figure representation clarification.

f. Please correct Figure 3 to accurately represent "**The third switch 228 is coupled to the computer system 208, the emulation input device 212 and the first switch 224 for conducting and transmitting the clock/data signal from the computer system 208 either to the real input device 210 or to the emulation input device 212 according to the control signal Cn.**" (Paragraph 0031). Based on Figure 3 the "third switch" 228 is coupled/connected to "210", "b1", "208", and the "forth switch". The "third switch" 228 and "first switch" 224 are not coupled/connected together in Figure 3.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Switch Control System and Method that Distinguishes Between a Plurality of Real and Emulation Input Devices".

6. The disclosure is objected to because of the following informalities:

a. Please replace "**The switch control system comprises a server 100, a real keyboard/mouse set 104, an emulation keyboard/mouse set 106, and a switch device 102 connected to the server 100, the real keyboard/mouse set 104 and the emulation keyboard/mouse set 106.**" (Paragraph 0005) with "The switch control system comprises a server 100, a real keyboard/mouse set 104, an emulation keyboard/mouse set 106, and a switch device 102 (connected to the server 100, the real keyboard/mouse set 104, and the emulation keyboard/mouse set 106)."

b. Please replace "**colliding with an emulation signal from**" (Paragraph 0006) with "colliding with an emulated signal from".

c. Please replace "**or to transmit/receive emulation signals**" (Paragraph 0009) with "or to transmit/receive emulated signals".

d. Please correct/define "**first detecting signal when OLE_LINK1a second acknowledge**" (Paragraph 0012).

e. Please correct/define "**the computer system is detected.OLE_LINK1**" (Paragraph 0012).

f. Please replace "real signals colliding with the emulation signals." (Paragraph 0025) with "real signals colliding with the emulated signals."

g. Please replace "**input device or to transfer emulation signals**" (Paragraph 0025) with "input device or to transfer emulated signals"

h. Please define acronym "**ACK**" (Paragraph 0028).

i. Please replace "**the logic device 214 comprises an AND gate, an OR gate or a**" (Paragraph 0030) with "the logic device 214 comprises of "AND" gates, "OR" gates, or a".

j. Please confirm that Figure 3 accurately represents the connections as outlined in Paragraph 0031.

k. Please define/elaborate the functional application of "a predetermined voltage level signal b_1 is a high-level voltage or a low-level voltage" (Paragraph 0031) in application to Figure 3 and the "Switch device" (Figure 2, 202).

l. Please replace "In such a scenario described above" (Paragraph 0036) with "In such a scenario as described above".

Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

7. Claims 1, 8, 11, 12, and 16 are objected to because of the following informalities:

   a. Please replace "**and then isolating signals of an unselected input device when the selected input device**" (Claim 1) with "and then isolating signals of an unselected input device when a selected input device" to resolve potential antecedent basis issues.

   b. Please replace "**a control device for selecting the real signal or the emulation signal**" (Claim 8) with "a control device for selecting the real signal or an emulation signal" to resolve potential antecedent basis issues.

   c. Please resolve objection (b.) above to resolve potential antecedent basis issue for "**transmitting either the real signal or the emulation signal according to a control signal**" (Claim 8).

   d. Please resolve objection (b.) above to resolve potential antecedent basis issue for "**emulation input device to receive the emulation signal**" (Claim 8).

   e. Please replace "**a first disabling signal to disable a third switch to the third switch so that the signal**" (Claim 11) with "a first disabling signal to

disable a third switch so that the signal" or correct to sentence structure of the claim to increase clarity.

f. Please replace "**a second disabling signal to disable a first switch to the first switch so that the signal**" (Claim 12) with "a second disabling signal to disable a first switch so that the signal" or correct to sentence structure of the claim to increase clarity.

g. Please replace "**scan_code_set**" (Claim 15) with "device interface protocol" for clarification purposes.

h. Please replace "**the communication interface for transmitting signal**" (Claim 16) with "the communication interface for transmitting a signal".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 17 recites the limitation "the control signal". There is insufficient antecedent basis for this limitation in the claim. Claim 17 is dependent on Claim 10, which reads, "outputting a first control signal to respond to the first detecting signal or a second control signal to respond to the second detecting signal respectively".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1- 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Thomas et al. (US 6,671,756 B1 December 30, 2003).

As per claim 1, Thomas et al. discloses, "A switch control system for a plurality of input devices" as **["A KVM switch having a uniprocessor architecture that accommodate multiple users and multiple computers" (Abstract) and Figure 8]**, "comprising a real input device and an emulation input device" **["the KVM switch also provides access to a user that is local to the switchbox and access to another user that is remote from the switchbox" (Column 2, Line 1), "The present embodiment uses a technique for emulating multiple computer channels concurrent with the processing of low priority software tasks and with the reception of keyboard and mouse peripheral data. This provides simultaneous clock generation for multiple channels of keyboard and mouse emulation" (Column 15, Line 12), Figure 3, and Figure 13]**, "the switch control system comprising: a switch device for selecting either of the two input devices" **[shown in FIG. 1. There, system 1 includes a KVM switch 2 (Column 3, Line 38)]**, "and then

isolating signals of an unselected input device when the selected input device is transmitting or receiving signals" **[The switch 2 ensures that only one workstation 3/7 enters data through the keyboard 5/9 or mouse 6/10 at any given moment, to avoid lock-ups. But, once the active workstation stops a keyboard and mouse activity, the other workstation can take control of the computer and enter data through its keyboard and mouse. Thus, both workstations 3 and 7 have immediate and shared access to all computers 13 (with the caveat that the switch 2 will prevent absolutely simultaneous data entries into the same computer at the same moment). (Column 6, Line 67)]**, "an instruction detecting device electrically connected to the switch device for detecting signals transmitted to the switch device" **[Signals from the workstation keyboard 5/9, mouse 6/10, and video monitor 4/8 of the workstations 3/7 are provided to the switch 37 via lines 25/26/27 (FIG. 5) and 11/12 (FIG. 1). The workstation signals are provided to the single processor 38. (Column 7, Line 49), Figure 8, and Figure 9]**, "and a control device electrically connected to the switch device and the instruction detecting device for receiving a detecting signal from the instruction detecting device and outputting a control signal to trigger the switch device and to control the selection of the switch device." **[Between the single processor 38 and the PCs 13 is a FPGA 41. Embodied in the FPGA is a computer I/O 42 providing input/output interfacing between the processor 38 and the PCs 13 (Column 7, Line 61), Figure 8, and Figure 9].**

As per claims 2 and 8, Thomas et al. discloses, "The switch control system of claim 1, wherein the signals comprise a real signal and an emulation signal" **["the KVM**

switch also provides access to a user that is local to the switchbox and access to another user that is remote from the switchbox" (Column 2, Line 1), Figure 3, and Figure 13], "the switch device comprises: a first switch coupled to the real input device for selecting the real signal;" **[(Figure 8, Index 3, 5, 6, 41, 42, 43, and 44)** and **(Figure 13, Index 4 and 68)]** "a second switch coupled to the first switch, the emulation input device, and the control device for selecting the real signal or the emulation signal and transmitting either of the two signals according to the control signal;" **[(Figure 8, Index 7, 9, 10, 41, 42, 43, and 44)** and **(Figure 13, Index 8, 69, and 43)]** "a third switch coupled to the emulation input device and the first switch for transmitting the signals either to the real input device or to the emulation input device according to the control signal when the second switch is triggered by the control signal;" **[(Figure 8, Index 3, 5, 6, 7, 9, 10, 41, 42, 43, and 44)** and **(Figure 13, Index 4, 8, 72, and 43)]** "and a fourth switch coupled to the first switch, the third switch and the real input device either for enabling the emulation input device to receive the emulation signal or for disabling the first switch so that the emulation input device is capable of receiving the real signal from the third switch according to the control signal." **[(Figure 8, Index 3, 5, 6, 7, 9, 10, 41, 42, 43, and 44)** and **(Figure 13, Index 4, 8 71, and 43)].**

It is the interpretation of the examiner that Thomas et al. discloses the usage of a processor in the application of a KVM (keyboard, video, mouse) switch. **[(Figure 8, Index 38, 39, 40, 41, 42, 43, and 44), (Figure 13, Index 4, 8, 43, 68, 69, 71, and 72), "Signals from the workstation keyboard 5/9, mouse 6/10, and video monitor 4/8 of the workstations 3/7 are provided to the switch 37 via lines 25/26/27 (FIG. 5) and**

11/12 (FIG. 1). The workstation signals are provided to the single processor 38. The processor 38 can, in an example embodiment, be a processor in the Siemens 167 family, such as the Siemens C163-16F processor." (Column 7, Line 49), "Between the single processor 38 and the PCs 13 is a FPGA 41. Embodied in the FPGA is a computer I/O 42 providing input/output interfacing between the processor 38 and the PCs 13" (Column 7, Line 61), and **"The microcontroller includes several I/O ports 50. Port0, Port1, and Port6 provide bi-directional communication from external devices to the CPU 46 via external bus 51 (Column 8, Line 57)].**

As a result the examiner has determined that the application of a processor (central processing unit (CPU) consisting of transistor switches, clock/data circuitry, and memory/registers) as equivalent to the claimed subject matter in reference to first, second, third, and forth switch as described in claim 2. Examiner holds the applicants discloser of

a. According to the preferred embodiment, the logic device 214 comprises an AND gate, an OR gate or a combination of other logic components. (Description, Paragraph 0030)
b. The first, the second, the third and the fourth switches 224, 226, 228 and 230 can be multiplexers or electronic switches. In addition, each of the above switches can have a corresponding output terminal connected with a register (not shown) for receiving output signals of the corresponding

switch as accurately as possible, so as to ensure that the clock/data signals are correct." (Description, Paragraph 0033)"

as evidence of the applicants intended "switch" structure/function/composition.

If applicant determines that the above evaluation/determination is in error, applicant is requested in response to this Office action to clearly and precisely outline the structural/functional difference between the processor structure detailed in Thomas et al. and applicants first, second, third, and forth switch.

As per claims 3 and 9, Thomas et al. discloses, "The switch control system of claim 2, wherein the four switches respectively comprise at least a multiplexer." As **[Syncs from the computers 13 are received by dual muxes 71 and 72 and placed on local and remote user sync buses. Local and remote muxes 68 and 69 will take syncs from either the sync buses (from the computers) or from the sync generation 43 for application to the local and remote monitors 4/8." (Column 23, Line 14)].**

As per claim 4, Thomas et al. discloses, "The switch control system of claim 1 further comprising: a logic device comprising a first input terminal coupled to the control device for receiving the control signals, a second input terminal, and an output terminal coupled to the switch device for outputting the control signal to the switch device; and a setting device coupled to the second input terminal of the logic device for setting operation modes of the logic device to trigger the switch device with the control signal." as **[Signals from the workstation keyboard 5/9, mouse 6/10, and video monitor 4/8 of the workstations 3/7 are provided to the switch 37 via lines 25/26/27 (FIG. 5)**

and 11/12 (FIG. 1). The workstation signals are provided to the single processor 38. The processor 38 can, in an example embodiment, be a processor in the Siemens 167 family, such as the Siemens C163-16F processor. The processor 38 may, in the example embodiment of FIG. 8, include FLASH memory and local RAM." (Column 7, Line 49) and **"Between the single processor 38 and the PCs 13 is a FPGA 41. Embodied in the FPGA is a computer I/O 42 providing input/output interfacing between the processor 38 and the PCs 13" (Column 7, Line 61)].**

As per claims 5 and 16, Thomas et al. discloses, "wherein the real input device and the emulation input device each comprises a PS/2 communication interface." as **[A cable from keyboard 5 is shown in FIG. 5 as PS/2 keyboard cable 25, which connects to keyboard port 26 of the switch 2. The mouse 6 employs PS/2 mouse cable 26, which is plugged into mouse port of switch 2 (Column 5, Line 46), (Figure 1, Index 5, 6,** and **15)**, and **(Figure 5, Index 25,** and **26)].**

As per claims 6 and 19, Thomas et al. discloses, "wherein the real input device is a mouse, a keyboard or a combination of both." as **[A cable from keyboard 5 is shown in FIG. 5 as PS/2 keyboard cable 25, which connects to keyboard port 26 of the switch 2. The mouse 6 employs PS/2 mouse cable 26, which is plugged into mouse port of switch 2 (Column 5, Line 46), (Figure 1, Index 5,** and **6)**, and **(Figure 5, Index 25,** and **26)].**

As per claims 7 and 20, Thomas et al. discloses, "wherein the emulation input device is the emulation of a mouse, a keyboard or a combination of both." as **["The KVM switch 2 also accommodates a second workstation 7 that may be relatively**

far from the KVM switch 2 (for example up to 500 feet away), which workstation 7 includes keyboard 9, mouse 10, and monitor 8." (Column 3, Line 43), "The switch 2 provides essentially unlimited support for different mouse types 6/10, different keyboard types 5/9, different monitor types 4/8, and different computer types 13. For example, the switch 2 is compatible with IBM PC/AT and PS/2 systems, SUN systems, etc. It is also compatible with VGA, SVGA, XGA and XGA-II video signals. PS/2 and SUN keyboards are accommodated, as are PS/2 Intellimouse, IBM ScrollPoint, Logitech Mouse Man+, Logitech Marble+, Logitech Marble FX, and Kensington Expert Mice, etc." (Column 3, Line 64), (Figure 1, Index 9, and **10),** and **(Figure 5, Index 25,** and **26)].**

As per claim 10, Thomas et al. discloses, "A switch control method for a plurality of input devices" as **["A KVM switch having a uniprocessor architecture that accommodate multiple users and multiple computers" (Abstract) and Figure 8]**, "comprising a real input device and an emulation input device" **["the KVM switch also provides access to a user that is local to the switchbox and access to another user that is remote from the switchbox" (Column 2, Line 1), "The present embodiment uses a technique for emulating multiple computer channels concurrent with the processing of low priority software tasks and with the reception of keyboard and mouse peripheral data. This provides simultaneous clock generation for multiple channels of keyboard and mouse emulation" (Column 15, Line 12), Figure 3, and Figure 13]**, "the switch control method comprising the steps of: executing an initialization process and setting parameters of a

communication interface for the input devices; **["An autoboot feature in the switch 2 boots all attached computers 13 during an initial power up or after a power failure. PCs 13 are booted transparently without any operator intervention and may be powered up one-at-a-time or all at once. Once the power stabilizes, a channel may be selected by a user of a workstation 3/7." (Column 4, Line 48)** and **"The switch 2 features mouse translation capability in which mouse types 6/10 may employ data protocols different from a designated computer 13, in which case the switch 2 translates the mouse protocol between the selected computer 13 and the mouse 6/10." (Column 4, Line 17)],** "transmitting/receiving a signal with a switch device according to the communication interface;" **["The microcontroller includes several I/O ports 50. Port0, Port1, and Port6 provide bi-directional communication from external devices to the CPU 46 via external bus 51" (Column 8, Line 57)**, and **(Figure 3, Index 17)]** "transmitting/receiving the signal with the real input device when the switch device is selecting the real input device and then isolating the real input device and the emulation input device;" **["The switch 2 ensures that only one workstation 3/7 enters data through the keyboard 5/9 or mouse 6/10 at any given moment, to avoid lock-ups. But, once the active workstation stops a keyboard and mouse activity, the other workstation can take control of the computer and enter data through its keyboard and mouse. Thus, both workstations 3 and 7 have immediate and shared access to all computers 13 (with the caveat that the switch 2 will prevent absolutely simultaneous data entries into the same computer at the same moment)." (Column 6, Line 67)**, and **(Figure 3,**

Index 3, 17, and 17)] "detecting the signal transmitted to or from the switch device with an instruction detecting device, and then outputting a first detecting signal once detecting that the real input device is responding or outputting a second detecting signal once detecting that the emulation input device is responding;" **["The switch 2 ensures that only one workstation 3/7 enters data through the keyboard 5/9 or mouse 6/10 at any given moment, to avoid lock-ups. But, once the active workstation stops a keyboard and mouse activity, the other workstation can take control of the computer and enter data through its keyboard and mouse. Thus, both workstations 3 and 7 have immediate and shared access to all computers 13 (with the caveat that the switch 2 will prevent absolutely simultaneous data entries into the same computer at the same moment)." (Column 6, Line 67), "Signals from the workstation keyboard 5/9, mouse 6/10, and video monitor 4/8 of the workstations 3/7 are provided to the switch 37 via lines 25/26/27 (FIG. 5) and 11/12 (FIG. 1). The workstation signals are provided to the single processor 38. The processor 38 can, in an example embodiment, be a processor in the Siemens 167 family, such as the Siemens C163-16F processor." (Column 7, Line 49)**, and **(Figure 8, Index 3, 5, 6, 7, 9, 10, 41, and 44)]**, "and outputting a first control signal to respond to the first detecting signal or a second control signal to respond to the second detecting signal respectively and switching the emulation input device to the real input device with the second control signal." **[The switch 2 ensures that only one workstation 3/7 enters data through the keyboard 5/9 or mouse 6/10 at any given moment, to avoid lock-ups. But, once the active workstation stops a keyboard and mouse activity, the**

other workstation can take control of the computer and enter data through its keyboard and mouse. Thus, both workstations 3 and 7 have immediate and shared access to all computers 13 (with the caveat that the switch 2 will prevent absolutely simultaneous data entries into the same computer at the same moment). (Column 6, Line 67), "Signals from the workstation keyboard 5/9, mouse 6/10, and video monitor 4/8 of the workstations 3/7 are provided to the switch 37 via lines 25/26/27 (FIG. 5) and 11/12 (FIG. 1). The workstation signals are provided to the single processor 38. The processor 38 can, in an example embodiment, be a processor in the Siemens 167 family, such as the Siemens C163-16F processor." (Column 7, Line 49), "Between the single processor 38 and the PCs 13 is a FPGA 41. Embodied in the FPGA is a computer I/O 42 providing input/output interfacing between the processor 38 and the PCs 13" (Column 7, Line 61), (Figure 3, Index 3, 7, 17, and 13), and **(Figure 8, Index 3, 5, 6, 7, 9, 10, 41, and 44)]**. Please also see the rejection to claim 2.

As per claim 15, Thomas et al. discloses, "wherein the step of selecting the real input device further comprising the step of recording values of the scan_code_set." as **["The switch 2 features mouse translation capability in which mouse types 6/10 may employ data protocols different from a designated computer 13, in which case the switch 2 translates the mouse protocol between the selected computer 13 and the mouse 6/10." (Column 4, Line 17), "The microcontroller includes several I/O ports 50. Port0, Port1, and Port6 provide bi-directional communication from external devices to the CPU 46 via external bus 51 and external instruction**

databus therebetween. Clark generation is provided via PLL 48 via either direct or pre-scaled clock input. Two multi functional general purpose timer ("GPT") units 55 and 56 are provided with 5 timers T2-T6. Each GPT unit 55/56 represents a flexible multi-functional timer/counter structure used for different time related tasks such as event timing, counting sync generation, etc. Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by asynchronize/synchronize serial channel ASC of USART 57 and by synchronize serial port SSP 49." (Column 8, Line 57), and **"The FLASH memory referred to previously (with respect to FIG. 8) is maintained in buffer 47, which communicates with the CPU 46 and the interrupt controller 52." (Column 8, Line 49)].**

As per claim 17, Thomas et al. discloses, "further comprising the step of receiving and outputting the control signal to trigger the switch device by a logic device." as **["Signals from the workstation keyboard 5/9, mouse 6/10, and video monitor 4/8 of the workstations 3/7 are provided to the switch 37 via lines 25/26/27 (FIG. 5) and 11/12 (FIG. 1). The workstation signals are provided to the single processor 38. The processor 38 can, in an example embodiment, be a processor in the Siemens 167 family, such as the Siemens C163-16F processor." (Column 7, Line 49)**, and **"Between the single processor 38 and the PCs 13 is a FPGA 41. Embodied in the FPGA is a computer I/O 42 providing input/output interfacing between the processor 38 and the PCs 13" (Column 7, Line 61), Figure 8**, and **Figure 9].** Please also see the rejection to claim 2.

As per claim 18, Thomas et al. discloses, "further comprising the step of setting operation modes of the logic device with a setting device." as **["Signals from the workstation keyboard 5/9, mouse 6/10, and video monitor 4/8 of the workstations 3/7 are provided to the switch 37 via lines 25/26/27 (FIG. 5) and 11/12 (FIG. 1). The workstation signals are provided to the single processor 38. The processor 38 can, in an example embodiment, be a processor in the Siemens 167 family, such as the Siemens C163-16F processor." (Column 7, Line 49)**, and **"Between the single processor 38 and the PCs 13 is a FPGA 41. Embodied in the FPGA is a computer I/O 42 providing input/output interfacing between the processor 38 and the PCs 13" (Column 7, Line 61), Figure 8**, and **Figure 9].** Please also see the rejection to claim 2.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 11, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al. (US 6,671,756 B1 December 30, 2003) and well known practices in the art.

As per claims 11,12, 13, and 14 applicant has generically claimed the application of a multiplexer circuit (implemented as an individual multiplexer or as cascading

multiplexers) in order to enable (select) one circuit output while disabling (deselecting) another circuit output. As a result it is obvious to one skilled in the art and general practices in the art that the structures and functions described in claims 11, 12, 13, and 14 are multiplexer circuits for the application/function of selecting an input and/or output signal.

Thomas et al. teaches the application of a processor in the application of a KVM switch, as **"The processor 38 can, in an example embodiment, be a processor in the Siemens 167 family, such as the Siemens C163-16F processor." (Column 7, Line 49)**, and as a result it is obvious to one skilled in the art and common practice in the art that multiplexer circuitry is integral in the application and functionality of processors in the selection of data input/output and the usage of control signals. The primary responsibility of a processor is to correctly select input signals, perform desired functions/signal manipulation, and correctly relay the results on the appropriate output signals. As a result a processor can obviously be considered a complex multiplexer.

Additionally applicant has failed to disclose in the specification/detailed description what construes a "switch" relative to composition and/or construction. As a result the examiner has applied the broadest interpretation of a "switch" and determined that a processor is within the scope of the term "switch" when applied to claims 11, 12, 13, and 14 relative to the application/function of a multiplexer circuit.

Conclusion

14. In addition to reference used under 35 U.S.C. 102, additional prior art references that disclose relevant subject matter on the merits can be found in Beard et al. (US 5,991,830 November 23, 1999.

a. Beard et al. teaches:

i. Multiple devices connected to single port of computer system.

ii. Data transfer between peripheral/computer system.

iii. Addressing peripheral.

iv. Port controller, port manager, and configuration manager.

v. PS/2 device connections for keyboard/mouse.

vi. Clock/data synchronization.

vii. STAR Concentrator/connector.

viii. Signal/Data isolation

15. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571) 272-9780. The examiner can normally be reached on Monday through Friday 9:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pierre M. Vital can be reached on (571) 272-4215. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 19, 2006
JRP

Jonathan R. Plante
ART UNIT 2112

PIERRE VITAL
SUPERVISORY PATENT EXAMINER